Abstract

A bus agent that may be used in an enhanced highly pipelined bus architecture. In one embodiment, the bus agent includes a target ready interface, a set of response interfaces for a set of response signals, and a data bus busy interface, and a bus clock interface for a bus clock signal. The bus agent of this embodiment also includes bus controller logic to track a plurality of transactions comprising a transaction N-1 and a transaction N, the bus controller being capable of asserting the target ready signal for transaction N if the bus agent is asserting the data busy signal for the transaction N-1 and deasserts the data busy signal.